CLAIMS:

1. An improved differential inverter (100) comprising a differential inverter (30) having

- a differential input for receiving a first pair of signals comprising a first input signal (DIN1) and a second input signal (DIN2)

- a differential control input for receiving a second pair of input signals comprising a first a first control signal (DC1) and a second control signal (DC2),

- a differential output for transmitting a third vector of differential signals comprising a first output signal (OUT1) and a second output signal (OUT2)

- said improved differential inverter (100) being characterized in that it further comprises a controlled bias generator (10) generating the second vector of input signals in response to a bias control signal (Cin) which is generated at an output of a voltage divider coupled to the differential output of the differential inverter (30) said bias control signal being indicative for a DC voltage of the of the differential output.

2. An improved differential inverter (100) as claimed in Claim 1 wherein the bias control signal (Cin) is generated in a coupling point (P) of a first resistor means (Ros1) to a second resistor means (Ros2) substantially equal to the first resistor means (Ros1), an end of the first resistor means (Ros1) and an end of the second resistor means being coupled to the differential output.

3. An improved differential inverter (100) as claimed in Claim 1 wherein the differential inverter (30) comprises a first transistor pair and a second transistor pair each of the transistor pairs comprising a n-type MOS transistor (T2) coupled to a p-type MOS transistor (T1) via a drain to drain connection, the n-type transistor (T2) having a first control terminal (G2) for receiving the second control signal (DC2) via a third resistor means (R3), the p-type transistor (T1) having a second control terminal (G1) for receiving the first control signal (DC1) via a fourth resistor means (R4).

4. An improved differential inverter (100) as claimed in Claim 1, 2 or 3 wherein the control bias generator (10) comprises a first CMOS inverter (11) coupled to a second CMOS inverter (12) and to a third CMOS inverter (13), the first CMOS inverter (11) receiving the bias control signal (Cin) and generating a variable control signal (VR) that is inputted to the second CMOS inverter (12) and to the third CMOS inverter (13), the second CMOS inverter (12) and the third CMOS inverter generating the second vector of input signals (DC1, DC2) in response to the variable control signal (VR).

5. An improved differential inverter (100) as claimed in Claim 4 wherein any of the CMOS inverters included in the controlled bias generator (10) comprises a pair of a p-type MOS transistor (T1') and a n-type MOS transistor (T2') said transistors being mutually coupled and having different geometrical properties A1' and A2', respectively.

6. A differential oscillator (400) comprising an improved differential inverter (100) as claimed in any claim from 1 to 5, said differential oscillator having a LC tank circuit (401) coupled between the terminals of the differential output of the improved differential inverter (100), the terminals of the differential output being cross-coupled to the differential input.